A PULSED-MEASUREMENT BASED ELECTROTHERMAL MODEL OF HBT WITH THERMAL STABILITY PREDICTION CAPABILITIES

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Abstract

In this paper, a new electrothermal non linear model of HBT suitable for CAD purposes is presented. This model is fully determined by pulsed measurement techniques and for the first time, it is shown that the prediction of thermal instabilities (collapse of current gain) is obtained from the CAD model. The model has been validated both by DC and RF load-pull measurements.

I - Introduction

Continuous technological improvements in the realization of GaInP/GaAs or AlGaAs/GaAs heterojunction semi-conductor devices lead to the rapid development of new generation of transistors. For power applications, HBTs have proven their capabilities of handling high power densities in the X-band and Ku-band. However, the working range of such devices is principally limited by thermal aspects [1]. These ones severely degrade RF performance or even can lead to the failure of the transistor. The mechanism responsible for this failure is known as the collapse of the current gain. Such phenomenon has been studied through the aid of physical considerations [2] and instability criteria have been derived. Because of the severe thermal limitations for HBT, electrothermal models of these devices are required for CAD purposes. The aim of this paper is to propose a new modeling approach of HBT based on pulsed I-V and pulsed [S] parameters measurements. This approach allows to fully characterize the device, to obtain the thermal resistance and for the first time it will be shown that the model obtained is able to predict the thermal stability behavior of multifingers transistors and to accurately simulate the collapse phenomenon, without any knowledge of the technological parameters. Moreover this approach remains valid for the prediction of the thermal stability of high power amplifiers where a number of transistors are placed in parallel in the output stage.

II - The characterization process

The characterization process relies on pulsed I-V and pulsed [S] parameters measurements [3] [4]. Short pulses of typical duration of 300 ns are applied both on the base and the collector of the transistor with a repetition period which can be varied from 8 µs to 100 µs, thus ensuring an isothermal characterization of the device. During the pulse duration, base and collector voltages and currents are measured simultaneously as well as the [S] parameters of the device in the 1 - 20 GHz frequency range. In order to obtain the electrothermal model, measurements are performed in 3 steps.

i) As the temperature of the junction is evaluated thanks to an electrical measurement, the first step of the characterization process is the calibration of the decrease of the base-emitter voltage for constant base current versus the temperature. To do that the transistor is placed in a thermal enclosure and constant base current pulses are applied for various temperatures. The base-emitter voltage is then measured and Vbe(T) characteristics are obtained for those base currents. Measurements made on GaInP/GaAs transistors have shown a constant slope $\left.\frac{\partial Vbe}{\partial T}\right|_{Ib} \approx -1.4 mV/°C$.

ii) The second step of the process is to perform I(V) and [S] parameters measurements for various temperatures. The temperature of the device can be fixed either through the thermal enclosure temperature or through the self-heating due to the quiescent bias from which pulses are issued. From these I-V and RF measurements, a non linear temperature dependent model can be extracted with the assumption that parasitic elements are temperature independent.

iii) The third step consists in performing DC measurements at a fixed collector-emitter voltage. So that the DC power dissipated in the transistor can be calculated as $Pdc = Vce_0 . Ic_0 + Vbe_0 . Ib_0$ (1). The DC Ic-Vbe characteristic is plotted and the intersection of

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this characteristic with the isothermal characteristics previously measured gives simultaneously the DC power and the temperature of the device. Then the thermal resistance of the device can be calculated for various temperature as $Rth = \frac{\Delta T}{\Delta Pdc} \quad (°C/W) \quad (2)$.

III - Characterization results and modeling

A large number of measurements have been performed on devices with various number (from one to ten) of emitter fingers. The transistors are GaInP/GaAs HBT processed at the Central Research Laboratory of Thomson-CSF [5]. Each emitter finger has an area of 2*30 μm^2 and both topologies with and without thermal shunt have been measured. Results concerning two and four emitter fingers without thermal shunt are presented here. In Fig. 1 the topology of the model adopted is shown together with the element equations. The thermal dependence of I-V characteristics have been described through the variation of the saturation currents Is, Isfe, Isfc while the intrinsic current gains β_F and β_R are assumed to be temperature independent. However, the external current gain Ic/Ib is temperature dependent. Fig. 2 shows the variation of those saturation currents versus temperature. These variations are modeled with an equation of the form

$$Is(T) = I_{ST0}.e^{\left(-\frac{Ts}{T}\right)} \quad (3),$$

where T is the junction temperature, I_{ST0} and T_S are fitting parameters. For the evaluation of RF performances the modeling of the Cbe capacitance is of prime importance and in order to obtain a coherent small signal – large signal description, the temperature dependence of Cbe capacitance must be taken into account. For that purpose, the Cbe values have been extracted from S-parameters at various temperatures and are shown in Fig. 3-a and 3-b for the junction and the diffusion capacitances respectively. It should be noticed the behavior of the Cbe(T) capacitance shown in Fig. 3-b obtained in DC conditions. Thermal resistance measurements can be obtained from the plots of isothermal and DC Ic-Vbe characteristics shown in Fig. 4 where the intersection points are shown in filled circled. From these plots the thermal resistance has been found to be 201, 202, 212, 218 °C/W at 56, 64, 75, 80 °C respectively.

IV - Model validation

The previous model have been checked both for DC and RF conditions. In DC conditions the ability of the CAD model to predict the current gain collapse has been investigated. For that purpose a distributed temperature model shown in Fig. 5 of a 2*(2*30 μm^2) fingers HBT has been obtained and implemented in various circuit simulation softwares. Results obtained for a fully symmetric circuit (Rth1=Rth2) have shown that the collapse of the current gain is not observed in the DC characteristics (Fig. 6). However a bifurcation analysis [6] of the DC characteristics reveals that a D-type bifurcation occurs for a value of Vce=7V (point D) as the determinant of the characteristic system cancels at this point. The remaining branch for higher Vce is then found to be unstable and the stable branch (Fig. 6) can be obtained through the use of a voltage probe [6] in parallel with Rth12. However, the stable branches can be obtained without the use of probe if a slight unbalance in thermal resistances is introduced in the circuit (Rth1≠Rth2). The resulting characteristics are shown in Fig. 7 and 8 compared with DC measurements[7]. We can observe the good agreement between measured and computed values obtained for this device. Finally RF power transfer characteristics have been simulated and compared to load pull measurements [8] at 10 GHz for a four fingers transistors with a good agreement demonstrating the capability of the electrothermal model to accurately predict the RF performances of the transistor (Fig. 9).

V - Conclusion

A non linear electrothermal model of HBT has been developed. This model has been obtained through pulsed I-V and [S] parameters measurements and has demonstrated good capabilities for the prediction of RF performances as well as thermal instability. It has also been shown that thermal instability known as current gain collapse corresponds to D-type bifurcation of the circuit and that in the case of symmetric structures can be numerically hidden. Further work will concern the investigation of the thermal stability in RF dynamic condition.

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References :

[1] – W. Liu
"Current Gain Collapse in Microwave Multifinger Heterojunction Bipolar Transistors Operated at Very High Power Densities"
IEEE, Trans. On Electron Devices, Vol.40, NO.11,Nov 1993

[2] – W.Liu, A.Khatibzadeh
"The Collapse of Current Gain in Multifingers Heterojunction Bipolar Transistors. Its substrate temperature dependence, Instability Criteria and Modeling",
IEEE Trans.On Electron Devices, Vol. 41, n°10, Oct 94, pp 1698-1707

[3] – J.P.Teyssier and al
"Fully Integrated Nonlinear Modeling and Characterization System of Microwave Transistors with On-Wafer Pulsed Measurements",
IEEE MTT-S digest, Orlando 1995, Vol 3,pp 1033-1036

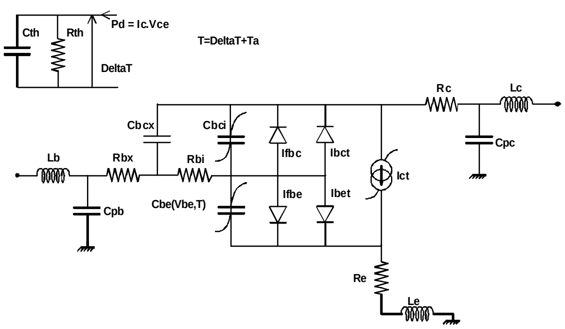
[4] – J.P.Viaud and al
"Nonlinear RF Characterization and Modeling of Heterojunction Bipolar Transistors under Pulsed Conditions"
EuMC Cannes 94, Vol.2, pp 1610-1615

[5] – S.L Delage and al
"Power GaInP/GaAs HBT MMICs"
EuMC Cannes 94, Vol.2, pp 1143-1148

[6] – R.Quéré and al
"Large Signal Design of Broadband Monolithic Microwave Frequency Dividers and Phase Locked Oscillator"
IEEE Trans.On MTT, Vol.41, N°11, Nov 93, pp 1928-1939

[7] – W.Liu
"Thermal Coupling in 2-fingers Heterojunction Bipolar Transistors"
IEEE Trans. On Electron Devices, Vol.42, NO.6, June 1995

[8] – F.Blache and al
"A Novel Computerized Multiharmonic Active Load-Pull System For the Optimization of High Efficiency Operating Classes In Power Transistors"
IEEE MTT-S digest, Orlando '95, Vol.3, pp 1033-1036



Ict = Ibe- Ibc

Ibe = Ise(T).exp(qVbe/Ne.k.T) ; Ibc = Isc(T).exp(qVbc/Nc.k.T)

Ibet = Ibe / βf ; Ibct = Ibc / βr ; Is(T) = Is_i(T).exp(- Ts_i/T)

Ibfe = Isfe(T).exp(q.Vbe / Nfe.k.T) ; Ibfc = Isfc(T).exp(q.Vbc / Nfc.k.T)

Cbn = Cjn0 / $(1\text{-}Vbn/\phi n)^{1/2}$ + Cdn(T).exp(q.Vbn / Nn.k..T) n = e, c

Fig. 1. Non-linear electrothermal model's HBT.

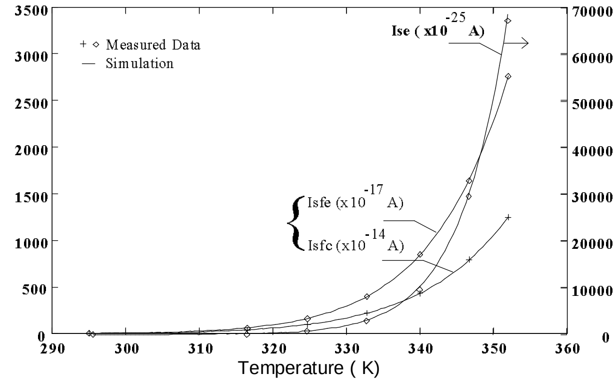


Fig. 2. Comparison between the measured and calculated saturation currents versus temperature.

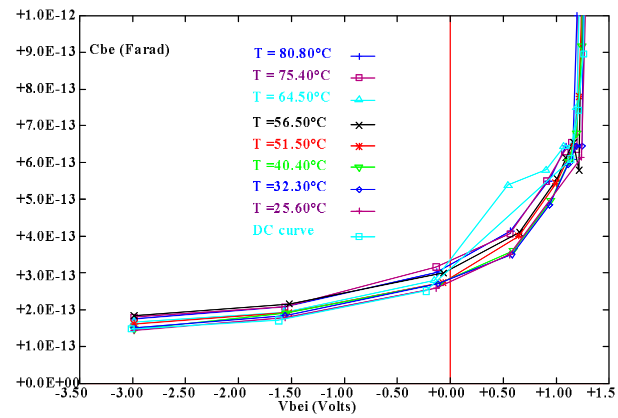


Fig. 3-a. Direct extraction from pulsed S-parameters of the junction capacitance Cbe at various temperature.

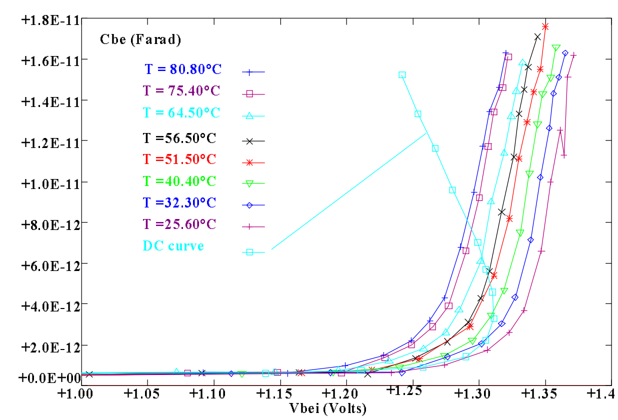


Fig. 3-b. Direct extraction from pulsed S-parameters of the diffusion capacitance Cbe at various temperature.

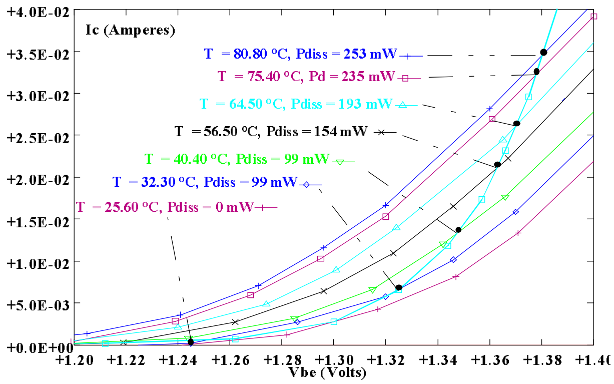


Fig. 4. Measured DC and pulsed at various temperature of Ic-Vbe characteristics et a Vce bias of 7V.

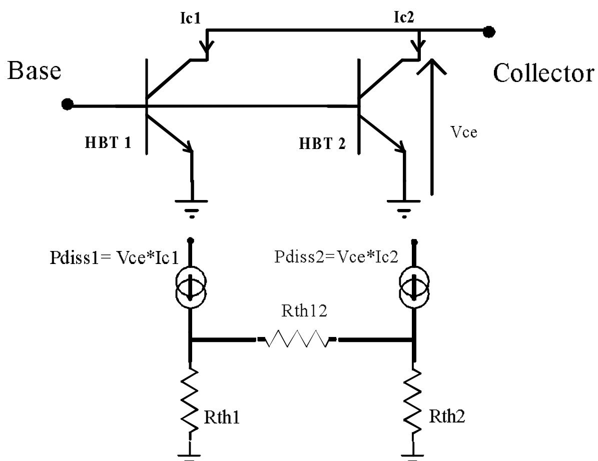


Fig. 5. Distributed temperature model of a 2*(2*30µm^2) fingers HBT.

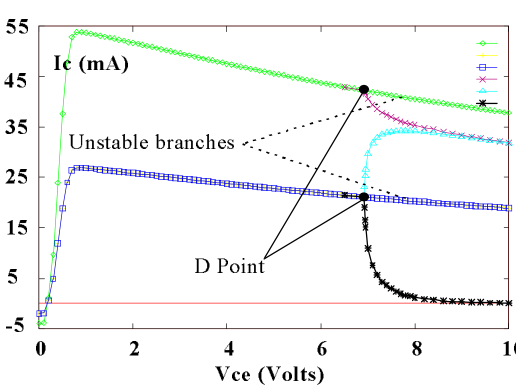


Fig. 6. Calculated plots of the total collector current and the collector currents in each fingers of an 2*(2*30µm^2) HBT when Rth1=Rth2=1200 °C/W (Ib = 4mA).

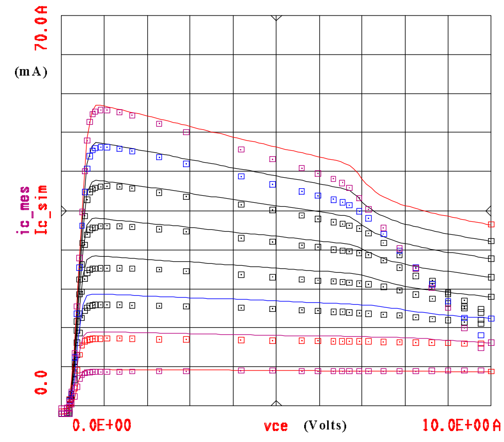


Fig. 7. Comparison between measured and calculated collector current Ic with the crunch effect of a 2*(2*30µm^2) fingers HBT (Ib = 0.5 mA/step).

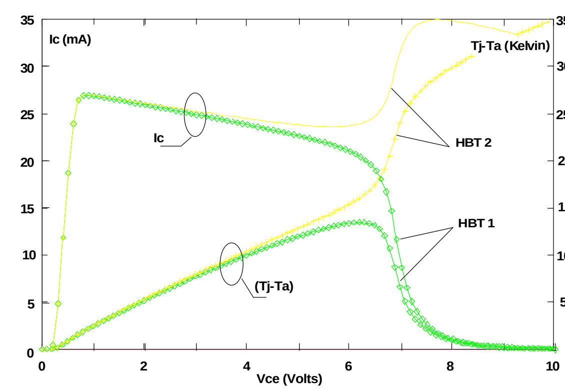


Fig. 8. Calculated plots of the collector current and (Tj-Ta) in each finger of an 2*(2*30µm^2) HBT when Rth1=1180, Rth2 = 1200 °C/W (Ib = 4 mA).

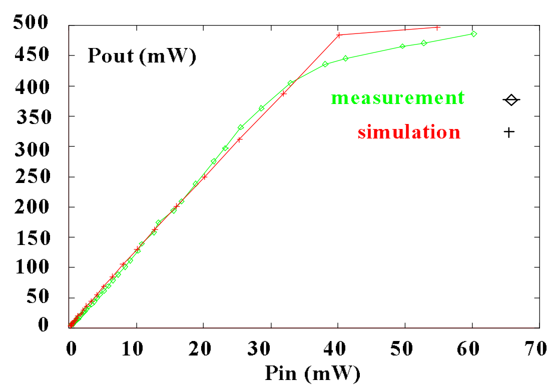


Fig. 9. Comparison between measured and calculated output power of a 4*(2*30µm^2) fingers HBT at 10 GHz.